Code No: RT22022 **R13** SET - 1

II B. Tech II Semester Regular Examinations, April/May - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1.	a)	Convert the decimal number 250.5 to base 3, base 4	(4M)
	b)	Write and prove de-Morgan laws	(4M)
	c)	Implement two input EX-OR gate from 2 to 1 multiplexer	(3M)
	d)	Write the demerits of PROM	(3M)
	e)	What is race around condition? How can minimized in J-K flip-flop	(4M)
	f)	write the difference between Mealy and Moore machine	(4M)

PART -B

2.	a)	Realize an 2 input EX-OR gate using minimum number of 2 input NAND gates.	(8M)
	b)	Subtract 278_{10} from 495_{10} using the excess-3 subtractor	(4M)
	c)	Encode the decimal numbers using 6, 3, 1,-1 weighted code. Is it a self-complementing code.	(4M)
3.	a)	Simplify the logic functions from binary to seven segment display code converter	(8M)
	b)	Simplify the following using Tabular method F(A , B , C , D , E) = Σ(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 2, 31)	(8M)
4.	a)	Draw the logic diagram 4-bit binary adder-subtractor circuit and explain its operation	(8M)
	b)	Design full adder from 3 to 8 decoder	(8M)
5.	a)	Design and implement Full adder with PLA	(8M)
	b)	Write the comparisons between PAL, PLA	(8M)
6.		What is a shift register? Draw the block diagram and timing diagram of a shift register that shows the serial transfer of information from register A to register B.	(16M)
7.	a)	The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x_2 changes from 0 to 1 while x_1=1. The output changes from 1 to 0 only when x_1 changes from 1 to 0 while x_2=1. Find a minimum row reduced flow table	(8M)
	b)	Draw a state diagrams of a sequence detector which can detect 101	(8M)

*****
~~~~~~

Code No: RT22022 **R13** SET - 2

II B. Tech II Semester Regular Examinations, April/May - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Convert the following numbers to decimal (4M)
   i) $(12121)_3$ ii) $(50)_7$
   b) Prove that $xy + x^1z + xy^1 = xy + x^1z$ (4M)
   c) Design half adder from 2 to 4 decoder (4M)
   d) Write the merits of PROM (3M)
   e) Write the difference counter and register (4M)
   f) What is Moore state machine diagram (3M)

PART –B

2. a) The message below has been coded in Hamming code. Decode the message for single error detection code (message = 4 bits).1001001 0111001 1110110 0011011. (8M)
   b) Design BCD code to Gray code converter. (8M)

3. a) Simplify the following using K-map method (8M)
   F(A , B , C , D , E) = Σ(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 31)
   b) Implement the following function with NAND gates (8M)
   F(x , y) = Σ(1, 2)

4. a) Define Multiplexer and explain the procedure to implement 32X1 MUX by Using 4X1 Multiplexers (8M)
   b) Design 4-bit digital comparator and explain with neat sketch (8M)

5. a) Implement f (A,B,C,D) = ∑(0,1,4,5,6,7,9,10,12,13,15) using PLA and explain its procedure (8M)
   b) Write the comparisons between PAL, PLA (8M)

6. a) Draw the circuit diagram of MOD-10 Counter and explain the operation of it (8M)
   b) What is race around condition and how to avoid it along with circuit diagram (8M)

7. a) Explain in detail the Mealy state diagram with one example (8M)
   b) Draw a state diagrams of a sequence detector which can detect 110 (8M)

*****
~~~~~~

Code No: RT22022 **R13** SET - 3

II B. Tech II Semester Regular Examinations, April/May - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Add the following numbers in give base without converting to decimal (4M)
   (i) $(1230)_4$ and $(23)_4$ (ii) $(296)_{12}$ and $(57)_{12}$
   b) Minimize below logic function with minimum number of literals (4M)
   $y\,(wz^1 + wz) + xy$
   c) Why do go for priority encoder rather than normal encoder (3M)
   d) Write the comparisons between PAL, PLA (4M)
   e) Write the differences between latch and flip-flop (4M)
   f) What is Mealy state diagram? (3M)

PART –B

2. a) Deduce X from the following? (8M)
   (i) $(BA0.C)_{16} = (X)_8$ (ii) $(10101100)_2 = (X)_{16}$
   (iii) $(FFE.C)_{16}=(X)_2$ (iv) $(7562)_8 = (X)_2$
   b) Subtract the following numbers using 10's complement (4M)
   (i) 5250 – 321 (ii) 753 – 864 (iii) 3570 – 2100 (iv) 20 – 1000
   c) Convert $(0011001.0101)_2$ to decimal and octal (4M)

3. a) Obtain the simplified expression in sum of products form using K-map method (8M)
   $F(A, B, C, D, E) = \Sigma(0, 1, 4, 5, 16, 17, 21, 25, 29)$
   b) Implement the following function with NAND gates (8M)
   $F(x, y, z) = \Sigma(0, 6)$

4. a) Implement $f(A,B,C,D) = \sum(0,1,3,5,6,8,9,11,12,13)$ using 8:1 MUX and explain its procedure (8M)
   b) Design and implement Full adder with two half adder and or gate (8M)

5. a) Implement $f(A,B,C,D) = \sum(0,1,3,5,6,8,9,11,12,13)$ using PROM and explain its procedure (8M)
   b) Write the merits and demerits of PROM (8M)

6. a) With the aid of external logic, convert D type flip-flop to a JK flip-flop. (8M)
   b) Design a synchronous modulo-12 counter using NAND gates and JK flip flops (8M)

7. a) Explain the state machine capabilities and limitations in detail (8M)
   b) Draw a state diagrams of a sequence detector which can detect 010 (8M)

*****
~~~~~~

Code No: RT22022 **R13** SET - 4

II B. Tech II Semester Regular Examinations, April/May - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

~~~~~~

PART –A

1. a) Write the first 10 numbers in base 4 (3M)
   b) Minimize below logic function with minimum number of literals (4M)
   $(x + y)(x + y^1)$
   c) Application of full adder (3M)
   d) Write the comparisons between ROM, PLA (4M)
   e) Write the difference between combinational circuit and sequential circuit (4M)
   f) Write the limitation of state machines (4M)

PART –B

2. a) Obtain the 1's and 2's complement of the following binary numbers (8M)
   1010101 , 0111000 , 0000001 , 10000 , 00000
   Also obtain 9's and 10's complement of the following decimal numbers
   09900 , 10000 , 00000
   b) What is a reflected code? Write about reflected codes by giving examples (8M)

3. a) Obtain the simplified expression for the Boolean function 'F' using don't care conditions 'd' in product of sums form (8M)
   $F = B^1DE^1 + A^1BE + B^1C^1E^1 + A^1BC^1D^1$
   $d = BDE^1 + CD^1E^1$
   b) Simplify the following function and implement it with NAND gates (8M)
   $F_1 = (B^1 + D^1)(A^1 + C^1 + D)(A + B^1 + C^1 + D)(A^1 + B + C^1 + D^1)$

4. a) Implement the following Boolean function with a multiplexer (8M)
   (i) $F(A, B, C, D) = \sum(1, 2, 5, 8, 6, 10,12,14)$ (ii) $F(A, B, C, D) = \sum(1, 2, 5, 6, 12)$
   b) Construct the 4 bit parallel adder with look ahead carry generation (8M)

5. a) Implement $f(A,B,C,D) = \sum(0,1,3,5,6,8,9,11,12,13)$ using PAL and explain its procedure (8M)
   b) Write the merits and demerits of PROM (8M)
~~~~~~

Code No: RT22022 **R13** SET - 4

6. a) What is flip-flop? How can be used in sequential circuit and explain in detail (8M)
   b) Explain about Master-slave flip-flop in detail (8M)

7. a) Reduce the number of states in the following state table and tabulate the reduced state table. (8M)

PS	NS_1Z	
	x=0	*x*=1
A	D, 0	H, 1
B	F, 1	C, 1
C	D, 0	F, 1
D	C, 0	E, 1
E	C, 1	D, 1
F	D, 1	D, 1
G	D, 1	C, 1
H	B, 1	A, 1

   b) Draw a state diagrams of a sequence detector which can detect 011. (8M)

*****